Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph bridging pages 1 and 2 (page 1, line 23 to page 2, line 3), with the following rewritten paragraph:

For example, in an example of the delay profile shown in Figs. 5A to 5C, when only one path is present, a shape of the path has a width as illustrated in Fig. 5A. On the other hand, when a plurality of paths are present, if paths have enough interval as shown in Fig. [[5]] 5B, a plurality of paths can be identified.

Please replace paragraph on page 2, 2nd full paragraph (lines 9-16), with the following rewritten paragraph:

In such case, in the prior art, it has been employed a method to set a minimum interval of respective finger position by omitting N samples (N is integer) before and after the detected path from next peak detection. Such method has been disclosed in "Path-Search Performance of ~~DS-WCDNA~~ DS-CDMA System in Laboratory and Field Experiments" (Aoyama et al.: Technical Report of IEICE, RCS 97-164, 1997-11) (hereinafter referred to as publication 1).

Please replace paragraph on page 9, 3rd full paragraph (lines 19-25), with the following rewritten paragraph:

A first correlated peak (path) can be obtained by outputting a maximum peak position and a peak level from the delay profile by the maximum value retrieving portion 13. The pattern generating portion 14 generates a logical pattern of the first correlated peak on the basis of the peak level and the peak position of the first peak obtained from the maximum value retrieving portion 13[[,]].

Please replace paragraph on page 10, 1st full paragraph (lines 1-9), with the following rewritten paragraph:

Upon detecting the second correlated peak, the subtractor 15 subtracts the logical pattern of the first correlated peak from the delay profile data in the delay profile storage portion 12 to prepare a profile ~~removing~~ from which is removed a correlated power of the first correlated peak and stores the prepared profile in the delay profile storage portion 12. It should be noted that the subtractor 15 may be replaced with other means, such as shift register or the like as long as the profile from which is removed the correlated power of the first correlated peak can be generated.

Please replace paragraph on page 10, 3rd full paragraph (lines 17-22), with the following rewritten paragraph:

The subtractor 15 subtracts the logical pattern of the second correlated peak from the delay profile data stored in the delay profile storage portion 12 to prepare the profile from which is removed the correlated power of the second correlated peak. Then, the prepared profile is stored in the delay profile storage portion 12.

Please replace paragraph bridging pages 12 and 13 (page 12, line 22 to page 13, line 2), with the following rewritten paragraph:

Upon detecting the second correlated peak, the subtractor 15 subtracts the logical pattern of the first correlated peak from the delay profile data in the delay profile storage portion 12 to prepare a profile ~~removing~~ from which is removed a correlated power of the first correlated peak and stores the prepared profile in the delay profile storage portion 12.

Please replace paragraph on page 13, 2nd full paragraph (lines 9-17), with the following rewritten paragraph:

The subtractor 15 subtracts the logical pattern of the second correlated peak from the delay profile data stored in the delay profile storage portion 12 to prepare the profile from which is removed the correlated power of the second correlated peak. Then, the prepared profile is stored in the delay profile storage portion 12. By repeating the foregoing operation for number of times, a plurality of correlated peak can be retrieved. It should be noted that the number of times is measured by the counter 16.

Please replace paragraph bridging pages 18 and 19 (page 18, line 17 to page 19, line 4), with the following rewritten paragraph:

Fig. 8 is a block diagram showing a construction of the maximum value retrieving portion of another embodiment of the multi-path detection circuit according to the present invention. In Fig. 8, another embodiment of the present invention has the same construction as the maximum value retrieving portion 13 in the former embodiment of the present invention shown in Fig. 3 except for a coefficient multiplying portion 71 is provided in the maximum value retrieving portion [[7]] 13. Like components to those in the former embodiment will be identified by like reference numerals and detailed description therefor will be omitted for avoiding redundant discussion and whereby to keep the disclosure simple enough to facilitate clear understanding of the present invention.

Please replace paragraph on page 19, 2nd full paragraph (lines 13-16), with the following rewritten paragraph:

In Fig. 8, the maximum value retrieving portion [[7]] 13 is constructed with the level comparing portion 13a, the selector 13b, buffer portion 13c, maximum position storage portion 13d and coefficient multiplying portion 71.

Please replace paragraph bridging pages 20 and 21 (page 20, line 25 to page 21, line 13), last paragraph, with the following rewritten paragraph:

It should be noted that the basic construction of another embodiment of the multi-path detection circuit according to the present invention is the same as the former embodiment of the multi-path detection circuit and the CDMA receiver shown in Fig. 1 and Fig. 2 according to the invention. Therefore, Like components to those in the former embodiment will be identified by like reference numerals and detailed description therefore will be omitted for avoiding redundant discussion and whereby to keep the disclosure simple enough to facilitate clear understanding of the present invention. [[ON]] On the other hand, the operation shown in Fig. 9 is realized by executing a program in the not shown control memory by the multi-path detection circuit 1. As the control memory, RON, IC memory or the like may be used.

Please replace the paragraphs on page 22, 1st and 2nd full paragraphs (lines 2-21), with the following rewritten paragraphs:

Thereafter, maximum value retrieval and maximum position retrieval are performed by the maximum value retrieving portion [[7]] 13 (steps S13 and S14 of Fig. 9). The maximum value retrieving portion [[7]] 13 outputs the path timing (correlated peak position) to the RAKE finger portion 5 (step S15 of Fig. 9). The pattern generating portion 14 generates the logical pattern of the detected peak on the basis of the maximum value and the peak position information detected by the maximum value retrieving portion [[7]] 13 (step S16 of Fig. 9).

The subtractor 15 subtracts the logical pattern generated by the pattern generating portion 14 from the delay profile data to remove the power component of the detected peak from the delay profile data (step S17 of Fig. 9). The delay profile storage portion 12 stores data from which is removed the power component of the detected peak from the delay profile data by the subtractor 15 (step S18 of Fig. 9). After completion of this process, the counter 16 is counted up (step 519 of Fig. 9). By repeating the foregoing process for the

times corresponding to number of fingers (step S20 of Fig. 9), necessary number of peaks can be detected.

Please replace the paragraph on page 23, 1st full paragraph (lines 2-10), with the following rewritten paragraph:

Fig. 10A shows an example of the delay profile in which a plurality of paths are located close proximity and levels of respective paths are substantially equal. In this case, in the maximum value retrieving portion 13 of the one embodiment of the present invention, difficulty is encountered in making judgment which sample is to be the first correlated peak, In contrast to this, in the maximum value retrieving portion [[7]] 13 of the shown embodiment, as the peak of the profile, the point at the left most position (detecting position 1) can be ~~sleeted~~ selected.

Please replace the paragraph on page 25, 1st full paragraph (lines 3-11), with the following rewritten paragraph:

The pattern generating portion 14 and the subtractor 15 in the detection objective pattern generating portion 81 perform generating operation of the delay profile data to be an object for detection. On the other hand, the sample detecting portion 83 performs similar operation as the prior art. [[IN]] In the further embodiment of the present invention, pattern generating operation by the pattern generating portion 14 and the subtractor 15 is performed only for the multi-path, in which the delay profiles overlap.